

QCC3084 VFBGA Hardware

Design Guide

80-41753-1 Rev. AA

September 8, 2022

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Revision history

Revision	Date	Description
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1 Introduction

This document describes the main points to consider when starting a design using QCC3084 VFBGA, with a particular focus on PCB layout and component selection. An example application schematic and lists of preferred components are provided in the appendix.

When designing a system using QCC3084 VFBGA, the board layout can influence end product performance. Qualcomm Technologies International, Ltd. (QTIL) recommends placing these printed circuit board (PCB) components in descending order of priority:

1. The switch-mode power supply (SMPS) components
2. Bluetooth® radio frequency (RF) trace and band-pass filter
3. Bluetooth RF decoupling
4. Crystal (XTAL)
5. Audio BGBYP capacitor
6. VDD_DIG decoupling
7. The quad serial peripheral interface (QSPI) flash devices and decoupling
8. All other decoupling

2 Power management

2.1 SMPS

QCC3084 VFBGA has two SMPSs, one for the system 1.8 V rail and one for the digital circuits. The 1.8 V SMPS output is 1.8 V typical and the digital SMPS changes between 0.7 V, 0.8 V, and 0.9 V depending on the power mode of the integrated circuit (IC). Both SMPSs have three modes of operation. The modes are automatically configured by QCC3084 VFBGA depending on the IC state:

1. The pulse width modulation (PWM)
2. The pulse frequency modulation (PFM)
3. Ultra low power (ULP), a lower power PFM mode

2.1.1 Components specification

A list of inductor and capacitor specifications is given in the appendix.

RELATED INFORMATION

[“Recommended SMPS components specification” on page 46](#)

2.1.2 Input power supply selection

QCC3084 VFBGA SMPS circuits can be powered from SMPS_VCHG or SMPS_VBAT using low impedance on chip switches to SMPS_DCPL. The typical impedance of the on chip VBAT switch is 600 mΩ and the VCHG switch is 1.2 Ω.

2.1.3 Minimize SMPS EMI emissions

A buck SMPS has two main current loops during operation, see [Figure 2-1](#) and [Figure 2-2](#). The first is active when the PMOS switch (S1) is closed. Current flows from the V_{IN} decoupling capacitor (C1) through the PMOS switch (S1), through the inductor (L1), and into the output capacitor (C2). As current always flows in a loop, the return path for the current is from the GND of C2 back to the GND of C1. On QCC3084 VFBGA the VIN net is SMPS_DCPL.

QCC3084 VFBGA has two SMPSs (1.8 V and the digital SMPS) with separate current loops.

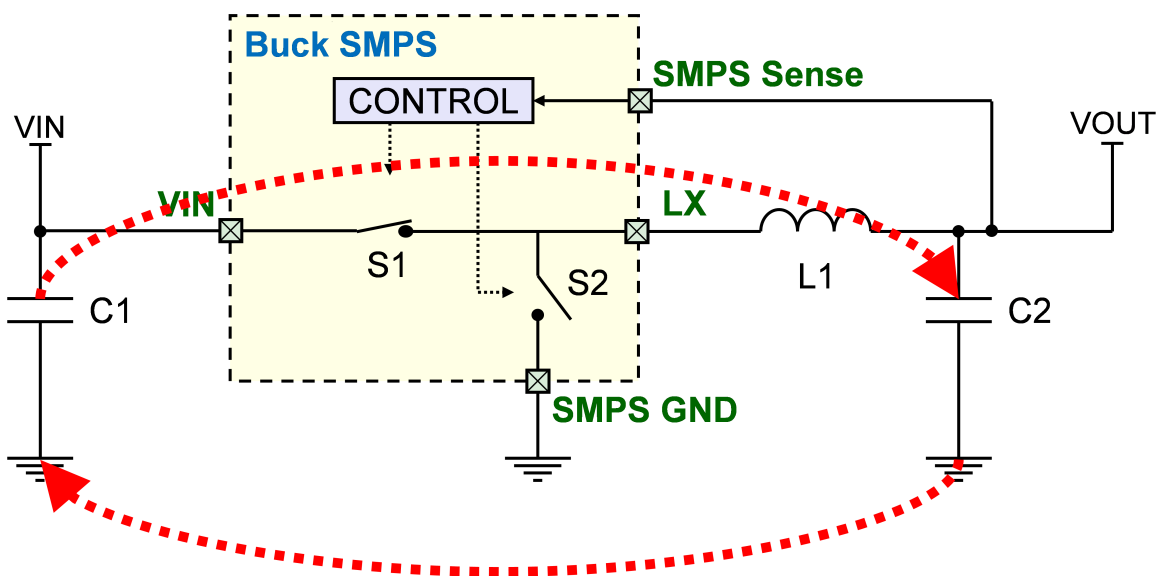


Figure 2-1 SMPS current loop - S1

Equation 2-1 shows the equation for an inductor.

$$V = L \times \frac{dI}{dt}$$

Equation 2-1 Equation for an inductor

When S1 is shut 'V' equals $V_{IN} - V_{OUT}$ (ignoring losses) and L is the fixed inductor value (4.7 μ H). This means that the inductor current increases linearly while switch S1 is closed.

The second current loop occurs when the PMOS (S1) opens and the NMOS (S2) is closed. When this happens the inductor carries on sourcing current *out* of the SMPS_GND node. Figure 2-2 shows that the return current is from the GND of C2 back to the SMPS_GND.

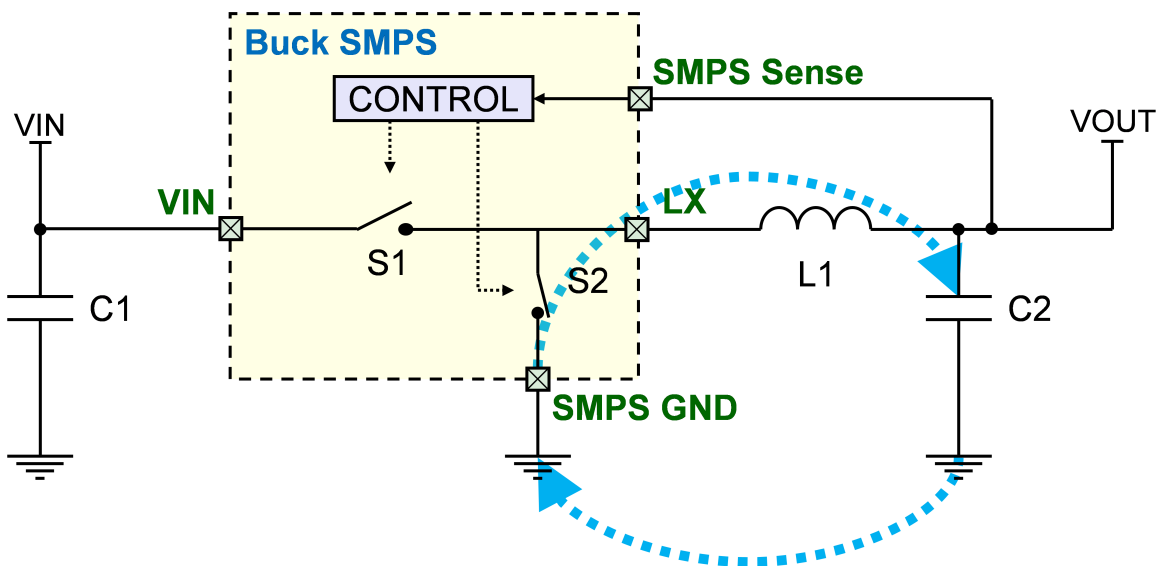


Figure 2-2 SMPS current loop - S2

The 'V' term in Equation 2-1 is $-V_{OUT}$ (ignoring losses) and L is still fixed. This means that dI/dt is now negative. While switch S2 is closed, the inductor current decreases linearly.

The QCC3084 VFBGA SMPS senses the current flowing in switch S2. If the inductor current reaches zero, switch S2 is opened to prevent the inductor current flowing in the reverse direction (from capacitor C2 to SMPS_GND). This is called discontinuous conduction mode (DCM), and increases SMPS efficiency in low load conditions.

In PFM and ULP modes, the SMPS frequency depends on the load current (typically several tens of kHz). In PFM/ULP mode, the inductor current (I_{LX}) starts at zero, ramps linearly to the max current when S1 is closed, and then ramps linearly back to zero when S2 is closed. However, there is a rapid change in the middle of the cycle when the current loop changes from [Figure 2-1](#) to [Figure 2-2](#).

[Figure 2-3](#) shows the voltage on LX and the SMPS PFM currents. I_{VIN} is the current when S1 is closed (sourced from SMPS_DCPL). I_{GND} is the current when S2 is closed (sourced from SMPS_GND).

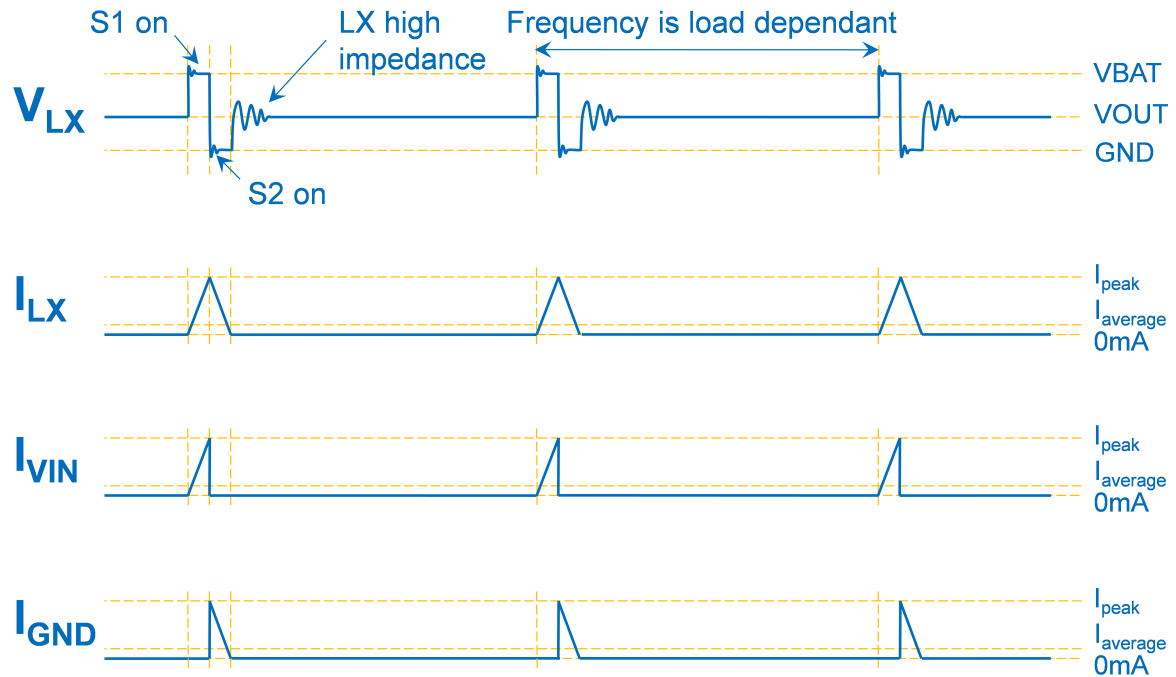


Figure 2-3 SMPS currents: PFM mode

The PFM peak current is ~350 mA on QCC3084 VFBGA. At the middle of the PFM cycle, 350 mA of current changes from [Figure 2-1](#) to [Figure 2-2](#). To maximize SMPS efficiency, S1 has to be turned off fast. With the typical switch capacitance and stray capacitance on the LX node, the voltage changes from V_{IN} to GND in <2 ns. This means that the SMPS emits electromagnetic interference (EMI) radiation from DC to several GHz.

In PWM mode, the SMPS operates with a typical frequency of 2.0 MHz. The voltage on the LX node changes between V_{IN} (SMPS_DCPL) and GND at 2.0 MHz as a square wave. Using [Equation 2-1](#), the inductor current is a triangle wave as shown in [Figure 2-4](#). Because QCC3084 VFBGA has a

discontinuous mode to increase efficiency at low loads, S1 and S2 both open if the inductor current drops to zero. This is not shown in Figure 2-4.

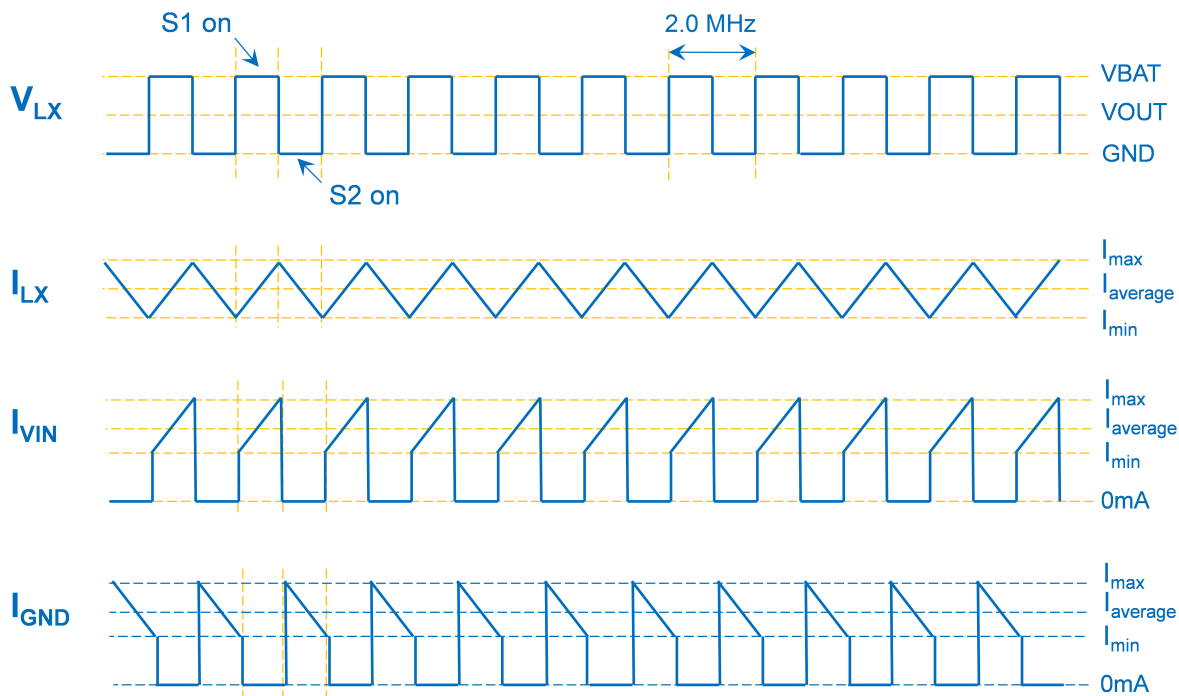


Figure 2-4 SMPS currents: PWM mode

SMPS_DCPL is connected to SMPS_VBAT or SMPS_VCHG using on-chip reverse current safe switches. The typical impedance of the on chip VBAT switch is 600 mΩ. The VCHG switch is 1.2 Ω. These switches form a low pass filter with the PCB decoupling capacitors on SMPS_VBAT and SMPS_VCHG. This prevents noise above ~300 kHz from coupling from the battery or charger power lines. A low impedance path should be provided from the SMPS_VBAT and SMPS_VCHG decoupling capacitors GND terminals back to the SMPS GND star point. Although it is not as important as the main SMPS current loops, the GND path will carry high frequency SMPS noise.

The placement of the SMPS_DCPL capacitor is important. The 2.2 μF capacitor must be placed as close as possible to the QCC3084 VFBGA device to close the high frequency current loop and minimize EMI. The 2.2 μF capacitor also reduces on-chip ringing caused by unwanted PCB inductances. If SMPS_DCPL is not properly decoupled to SMPS_GND, the EMI from the SMPS is higher, and in the worst case the resulting transient voltage spikes could damage QCC3084 VFBGA.

Figure 2-5 shows the ideal SMPS layout for QCC3084 VFBGA. The input capacitor for both SMPS is C13 (SMPS_DCPL pin). The inductor/capacitor for the 1.8 V and digital SMPS are respectively L1/C1 and L2/C2. The SMPS current loops are kept as small as possible to minimize EMI from the SMPS. The 1.8 V and digital outputs are taken from the capacitors to minimize high frequency noise on the power rail. The capacitor grounds are firmly connected to the main PCB GND plane (metal layer L2) to ensure that the power rails are referenced by the main PCB GND.

There should not be any tracks below the two LX tracks and the LX inductor pads. Also ideally, sensitive PCB traces should not be routed near any of the SMPS components or PCB traces.

In this layout, the two inductors (L1 and L2) use a 0806 (imperial) package, DFE201610E-4R7M=P2 from Murata. This inductor meets the saturation current specification in Table B-1. Provided that the

capacitor voltage derating can meet the specifications provided in [Table B-3](#), 0402 (imperial) capacitors can be used for C1 and C2.

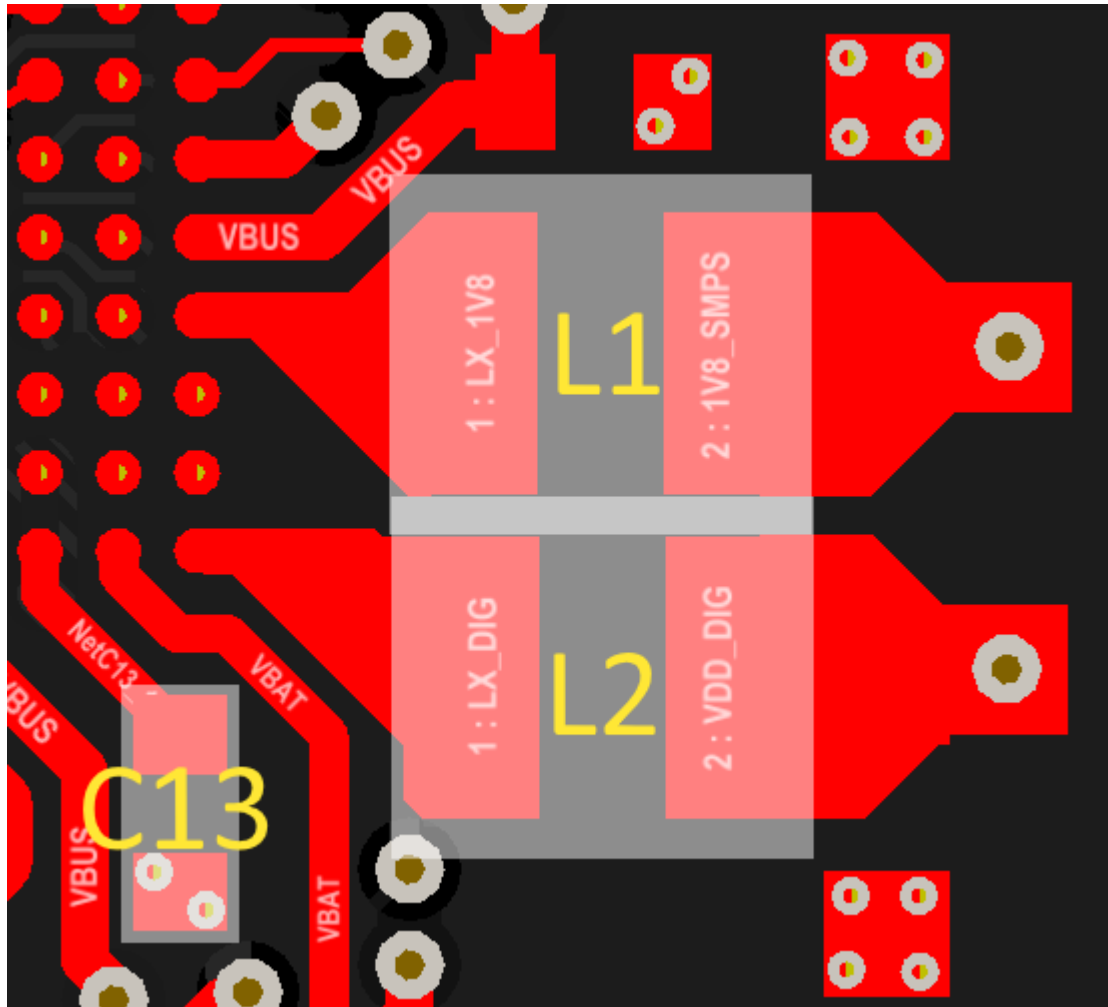
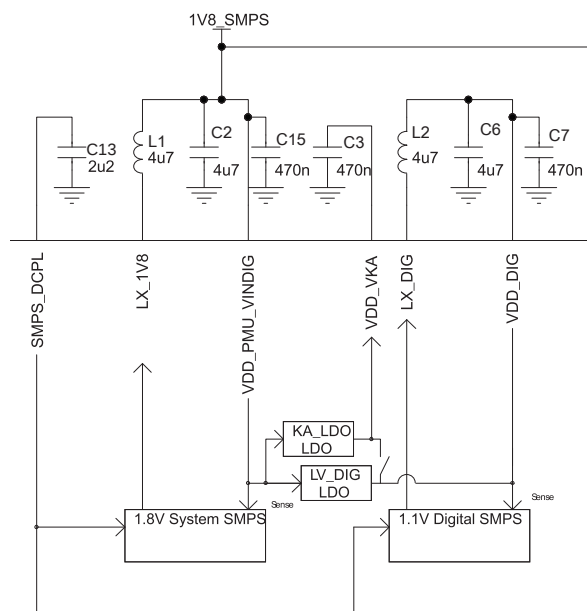


Figure 2-5 QCC3084 VFBGA SMPS Layout

[Figure 2-6](#) shows the corresponding PCB schematic.

NOTE C15 and C7 are intended to decouple VDD_PMU_VINDIG and VDD_DIG, and should be placed as close as possible to those pins. For more information, see [Internal LDOs and digital core decoupling](#).



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Figure 2-6 SMPS PCB schematic

Figure 2-7 shows the S1 current loop created in the 1.8 V SMPS when the PMOS switch is closed. The current loop is closed by the 2.2 μ F capacitor flowing in the GND plane.

The placement of C13 close to the chip is critical to limit the voltage spikes on SMPS_DCPL caused by PCB inductance.

The area within the current loop should be minimized by placing the SMPS components as close as possible to QCC3084 VFBGA.

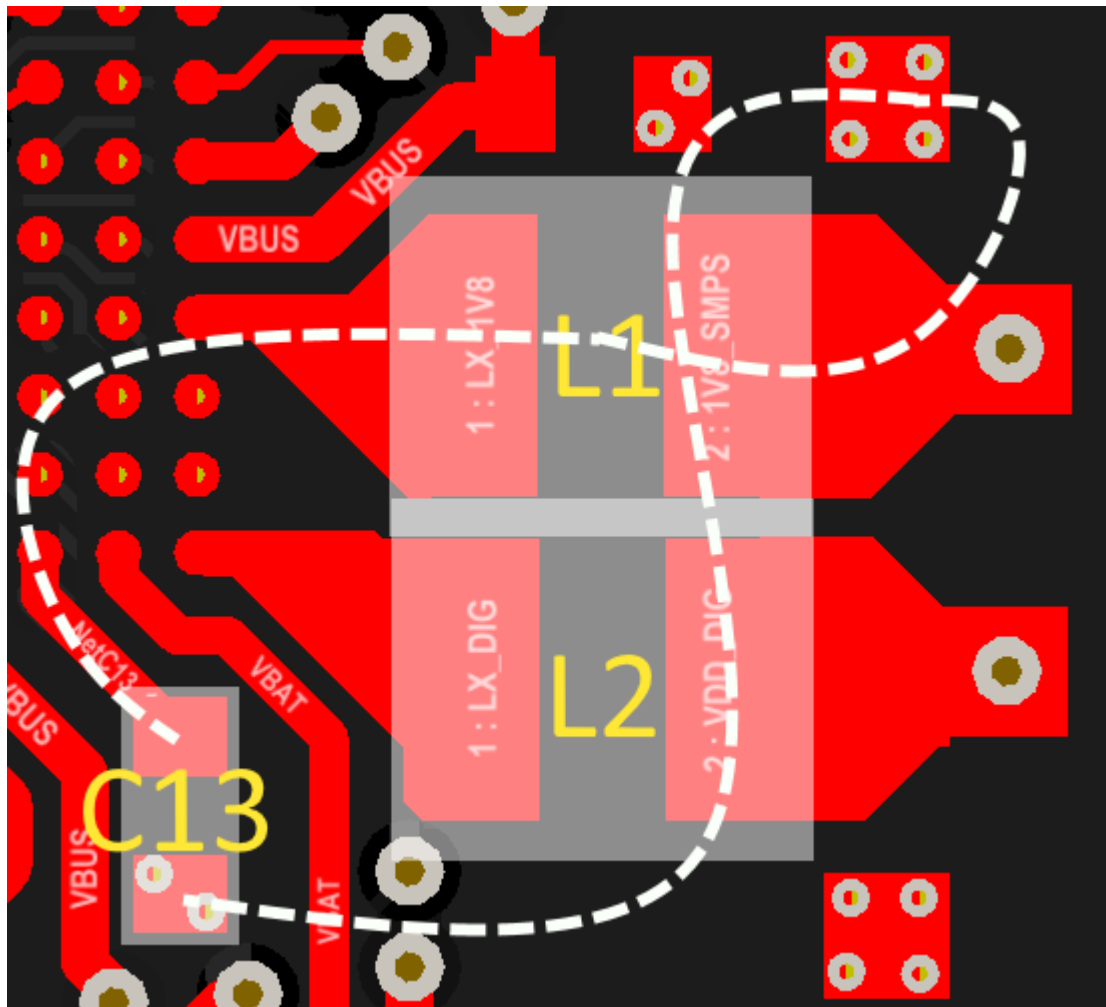


Figure 2-7 1.8 V SMPS S1 current loop

Figure 2-8 shows the S2 current loop for the 1.8 V SMPS created when the NMOS switch is closed. In PFM mode, the S1 current has reached ~350 mA before the start of the S2 loop. To minimize EMI, this loop should be kept as small as possible.

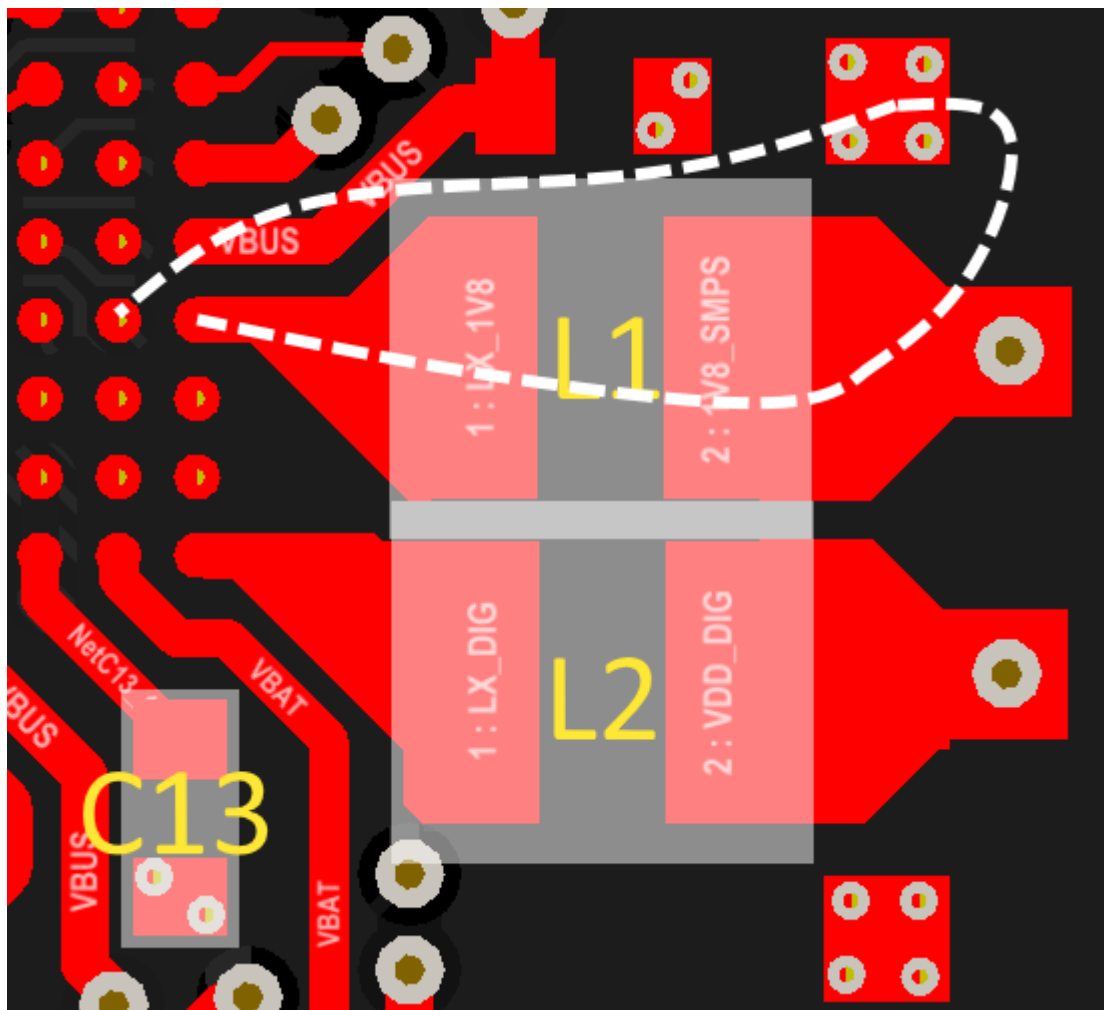


Figure 2-8 1.8 V SMPS S2 current loop

Similar current loops occur for the digital SMPS (involving C13, L2, and C2). Similar to the 1.8 V SMPS, the loop should be kept as small as possible.

To minimize peak currents taken from SMPS_DCPL, the 1.8 V and digital SMPS are clocked 180° out of phase from each other.

2.1.4 Internal LDOs and digital core decoupling

There are three internal LDOs connected to the VDD_PMU_VINDIG pad. A 470 nF capacitor must be connected very close to it.

The Digital Core supply is taken from the VDD_DIG pad. Another 470 nF capacitor must be connected very close to it.

2.1.5 Powering external components

A current of up to 100 mA can be drawn from the 1.8 V SMPS to power external components.

Depending on the maximum current, configuration of QCC3084 VFBGA may be required, see [Table 2-1](#).

Table 2-1 Configuring QCC3084 VFBGA to power external components from 1.8 V SMPS

Max. current	Condition required	How to enable
<30 mA	Supported in the default configuration.	-
<100 mA	The SMPS must be in the PFM/PWM mode.	The device should not be in Deep Sleep mode to ensure the SMPS remains in PFM/PWM mode. ^a

^a To disable Deep Sleep mode an application should use the `VmDeepSleepEnable(bool enable)` trap API.

2.2 Charger

The QCC3084 VFBGA charger has two circuit configurations with different charge current capabilities:

- Internal configuration: Supports lower charge rates with no additional external components required.
- External configuration: Supports higher fast charge rates with the addition of one PNP pass device and external resistor. Lower trickle and Pre-charge charge currents are still available in External configuration.

2.2.1 Charger connections

Internal charger configuration

[Figure 2-9](#) shows that in internal configuration, the VCHG_SENSE pin is tied to VCHG and CHG_EXT is left unconnected. The charge current passes through QCC3084 VFBGA internally in all states.

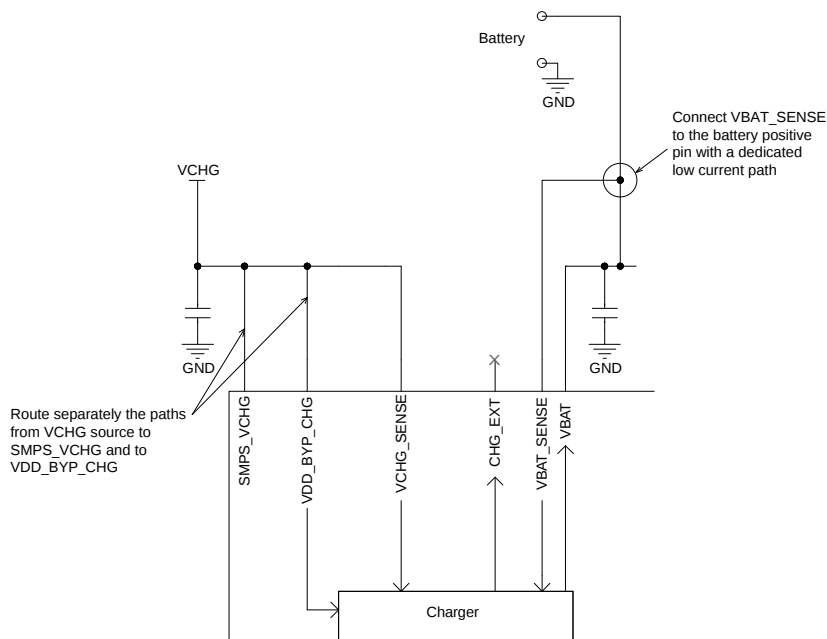


Figure 2-9 Schematic of internal charger configuration

Charge current enters through the VDD_BYP_CHG pin, and the VCHG net should be locally decoupled with a 2.2 μF ceramic capacitor. As the VCHG net is a high-voltage node, the capacitor must be appropriately voltage rated. QTIL recommends use of a capacitor rated for at least 10 V.

The charger output current exits via the VBAT pins to the battery. VBAT should be locally decoupled with a 2.2 μ F ceramic capacitor.

The VBAT_SENSE pin is used to sense the voltage on the battery and be routed as a Kelvin connection (separately) to the battery connector. This Kelvin connection avoids the IR drop in the battery PCB traces, which can lead to early termination, from affecting the charge process. As this is a sense connection, thick PCB tracks are not required.

Charge current can be up to 200 mA in this configuration, therefore VDD_BYP_CHG and VBAT PCB tracks must be suitably sized to carry the charge current.

External charger configuration

External charger configuration, see [Figure 2-10](#), is used for when higher charge currents are required. It requires an external PNP pass transistor and a sense resistor.

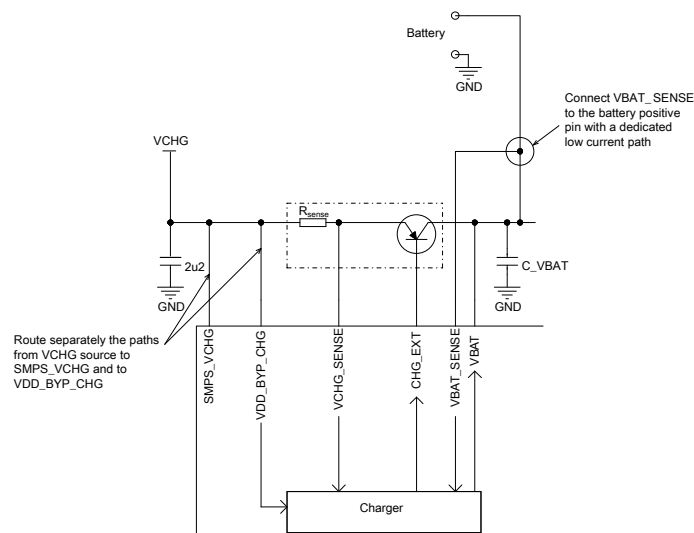


Figure 2-10 Schematic of external charger configuration

In this configuration, QCC3084 VFBGA monitors the voltage sensed across a sense resistor R_{sense} and sinks current into CHG_EXT to control the external transistor. The charger system is powered from the VCHG pin, which should be locally decoupled with a 4.7 μF ceramic capacitor (C_VBAT).

As for Internal configuration, the VCHG net should be locally decoupled with a 2.2 μ F ceramic capacitor. As the VCHG net is a high-voltage node, the capacitor must be appropriately voltage rated. QUIL recommends use of a capacitor rated for at least 10 V, and VBAT locally decoupled with a 2.2 μ F ceramic capacitor.

VCHG_SENSE should be connected directly to the R_{sense} resistor. Because this is a sense connection, thick PCB tracks are not required. The VCHG pin should also connect to the R_{sense} resistor. This will ensure accurate measurement of the voltage across R_{sense} .

The VBAT_SENSE pin is used to sense the voltage on the battery and routed as a Kelvin connection (separately) to the battery connector. This Kelvin connection avoids the IR drop in the battery PCB traces, which can lead to early termination, from affecting the charge process.

In the fast charge phase, the charge current is routed through pass transistor and fast charge current can be up to 1.8 A in this configuration. Therefore, the R_{sense} resistor, external transistor, and battery connecting PCB tracks must be suitably sized to carry the charge current. Trickle and Pre-charge currents flow internally through QCC3084 VFBGA. Therefore, VCHG and VBAT PCB tracks should be suitably sized to carry the charge current in these phases.

The CHG_EXT pin can sink up to 100 mA and should be suitably sized.

Because of the higher currents, PCB routing becomes more critical. Figure 2-11 shows the ideal tracking around the VDD_BYP_CHG pin.

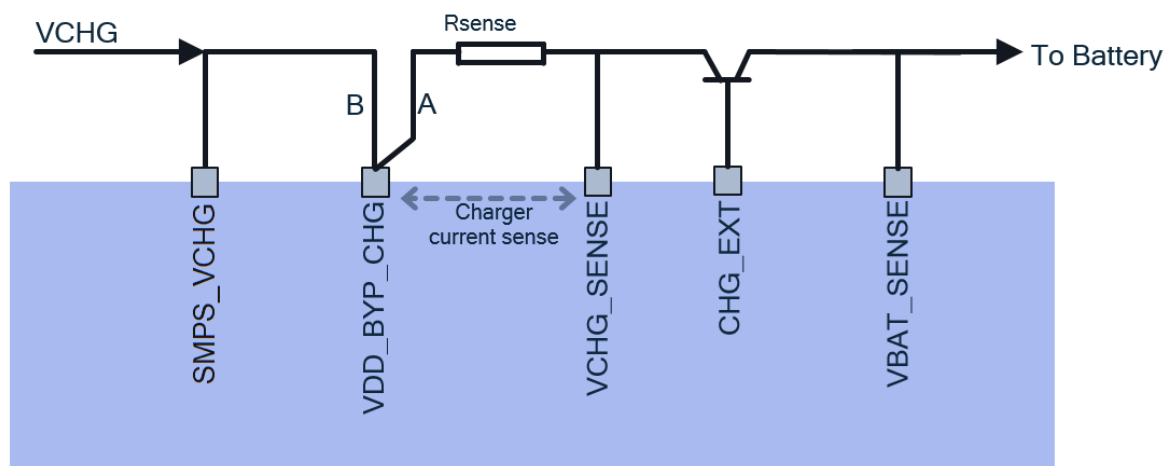


Figure 2-11 Ideal tracking around VDD_BYP_CHG pin

A common cause of problems with charge current accuracy is due to the PCB routing around the VDD_BYP_CHG pin and sense resistor. When the internal power switch is configured for the VDD_BYP regulator to be powered from VCHG, any current drawn by this regulator also flows into the VDD_BYP_CHG pin. The above routing minimizes any IR voltage from the VDD_BYP current from appearing in the charger systems sensing of the charge current, any sharing of tracks A and B will lead to a small increase in battery charge current depending on VDD_BYP current.

It is also important that the VCHG supply is routed as above, and not routed to R_{sense} first, as this also adversely affects charge current.

NOTE The QCC3084 VFBGA monitors the voltage between the VDD_BYP_CHG and VCHG_SENSE pins. This controls the charge current.

Excessive PCB impedance in the track marked A appears as additional R_{sense} resistance to the QCC3084 VFBGA and leads to lower than expected charge current.

Pass transistor choice

The H_{fe} (current gain) of the pass transistor must be between 45 and 700. High gain or Darlington devices are not suitable and lead to poor current control.

When choosing transistors, note that transistor H_{fe} values are usually quoted with 2 V V_{ce} . At low VCHG-VBAT headroom V_{ce} can fall well below this value. In this state QCC3084 VFBGA safely limits the maximum base current, and charge current is reduced.

Because significant heat can be dissipated within pass transistor, it is vital to select a device package capable of dissipating the heat generated within the device. PCB design must allow sufficient

heatsinking of external transistor, into the board and environment, enabling the device to remain within its Data Sheet ratings.

Power dissipation in external transistor, is at its greatest at the V_{fast} transition point and maximum VCHG voltage. At this point, the voltage across the transistor is at its highest, and the current is also at its highest.

Peak Power dissipation in pass transistor (W) = $(VCHG_{max} - V_{fast}) * I_{fast}$

Sense resistor choice

The sense resistor determines maximum fast charge current. QUIL recommends devices with a tolerance of 1% or lower are used to ensure accurate charge current. The resistor must be capable of dissipating heat generated within it during fast charge operation.

In external configuration, the target R_{sense} voltage is selectable between 100 mV and 10 mV in < 1 mV steps. The R_{sense} value should be chosen using [Equation 2-2](#).

$$I_{fast(EXT)} (A) = 0.1 (V) / R_{sense} (\Omega)$$

Equation 2-2 Equation for an R_{sense} value

For example, a 56 m Ω resistor gives an $I_{fast(EXT)}$ maximum of ~1.78 A, adjustable in approximately 1 mA steps down to the minimum of 200 mA..

To guarantee a particular max current, a PCB designer should allow for 1% tolerance in the external charger circuit, and resistor tolerance of typically 1%. That is, for 1 A max the total resistance should be 100 mR x 2% = 102 mR.

VBAT capacitance

The capacitance required on the VBAT net (C_{VBAT}) is different between Internal and External Configuration. See *QCC3084 VFBGA Data Sheet* (80-41752-1) for the required VBAT net capacitance.

2.2.2 General charger operation

For information on general charger operation, see *QCC3084 VFBGA Data Sheet* (80-41752-1).

2.3 SYS_CTRL

SYS_CTRL is VBAT tolerant (4.8 V max), and typically connected via a button to VBAT. SYS_CTRL has no internal pull resistor, and requires an external pull-down if left undriven.

When connected using a button to VBAT a series 100 k Ω resistor should be added, see [Figure 2-12](#). When driving SYS_CTRL from another IC the minimum series resistance required is 50 Ω .



Figure 2-12 SYS_CTRL connected to 100 k Ω resistor in series

For additional information on SYS_CTRL, see *QCC3084 VFBGA Data Sheet* (80-41752-1).

2.4 Powering microphones

Microphones can be a significant contributor to system power consumption. As sensitive analog components ensuring the correct supply is used can be critical to achieving good performance.

Typically the microphones used with QCC3084 VFBGA are either micro electro mechanical system (MEMS) or ECM. MEMS microphones can be divided into those with an analog or digital pulse-density modulation (PDM) interface.

To minimize power consumption, it is generally a requirement to put microphones into a low power state when not in use. In the case of analog microphones this is typically by removing power to them. Digital MEMS microphones often feature a low power suspend mode which is activated when the clock supplied by the host is below a specified frequency. Where the supply current in the suspend mode is significant digital MEMS mics may also require the supply to be removed when they are not in use.

2.4.1 Microphone Power supply recommendations

2.4.1.1 ECMs

The integrated mic bias regulator is recommended for supplying ECMs. This can be enabled under software control and has been designed to meet the low power supply noise requirements of ECMs.

RELATED INFORMATION

[“QCC3084 VFBGA example application schematic and BOM” on page 42](#)

2.4.1.2 MEMS microphones

The power supply rejection performance of MEMS microphones varies widely although it is generally much higher than ECMs.

The following supply options are typically available in the QCC3084 VFBGA designs:

- Mic bias regulator
- 1.8 V SMPS
- External low dropout regulators

To minimize system power consumption, it is generally desirable to power MEMS mics from the 1.8 V SMPS. If this option is selected, it is critical to ensure that the mic has sufficient power supply rejection. The ripple on the supply to the microphones can be reduced by adding an RC low pass filter between the 1.8 V rail and mics. QUIL recommends that this filter is before any supply switches as shown in [Figure 2-13](#) to limit inrush current when the mics are enabled. C1 should be 4.7 μ F maximum and R1

chosen to ensure that with the minimum specified output of the SMPS (excluding glitches) the minimum voltage requirement of the microphone can be satisfied. A good starting point is 10 Ω .

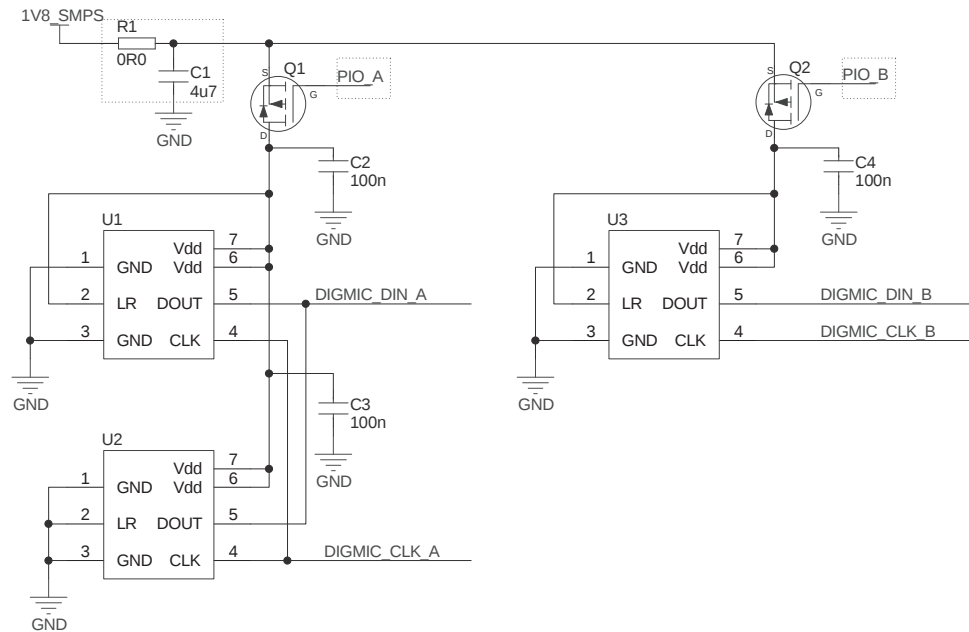


Figure 2-13 RC low pass filter between 1.8 V rail and mics

The mic bias regulator can also be used to power MEMS mics.

NOTE For stability the mic bias regulator requires a 10 Ω series resistor before any capacitors (the maximum capacitive load with 10 Ω is 2.2 μ F). For more details, see *QCC3084 VFBGA Data Sheet* (80-41752-1).

If additional switched microphone supplies are required, external low dropout regulators supplied from the battery with an enable input can be used.

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3 Bluetooth radio

3.1 RF PSU component choice

QCC3084 VFBGA has one integrated LDO to power the Bluetooth subsystem.

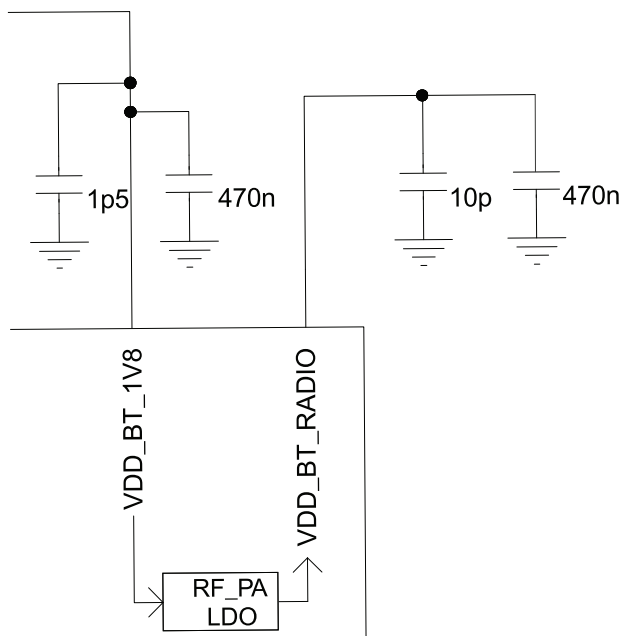


Figure 3-1 RF power supply arrangement

QTI recommends use of multilayer ceramic capacitors for the decoupling capacitors. The 1.8 V input to VDD_BT_1V8 should be decoupled with 470 nF and 1.5 pF capacitors. The 1.5pF capacitor should be placed as close as possible to the VDD_BT_1V8 pin.

The output of the LDO should be decoupled with 470 nF and 10 pF directly on the terminal, as shown in [Figure 3-1](#). The RF decoupling cap in particular (10 pF, C11) is strongly recommended to be placed very close to the VDD_BT_RADIO pin to minimize the loop inductance at RF frequencies.

wy1525676223645.2

3.2 RF filter

In order to meet statutory emissions limits, a band pass filter is typically required between the RF terminal and antenna to reduce out of band emissions. Either an integrated (for example, low temperature co-fired ceramic (LTCC) and surface acoustic wave (SAW)) or a discrete components filter can be used. [Figure 3-2](#) shows an example of the integrated filter. For recommended filter specification and example components, see *Related Information*.

An additional antenna matching network may be required between the filter and antenna. The design of such a network is not discussed in this document.

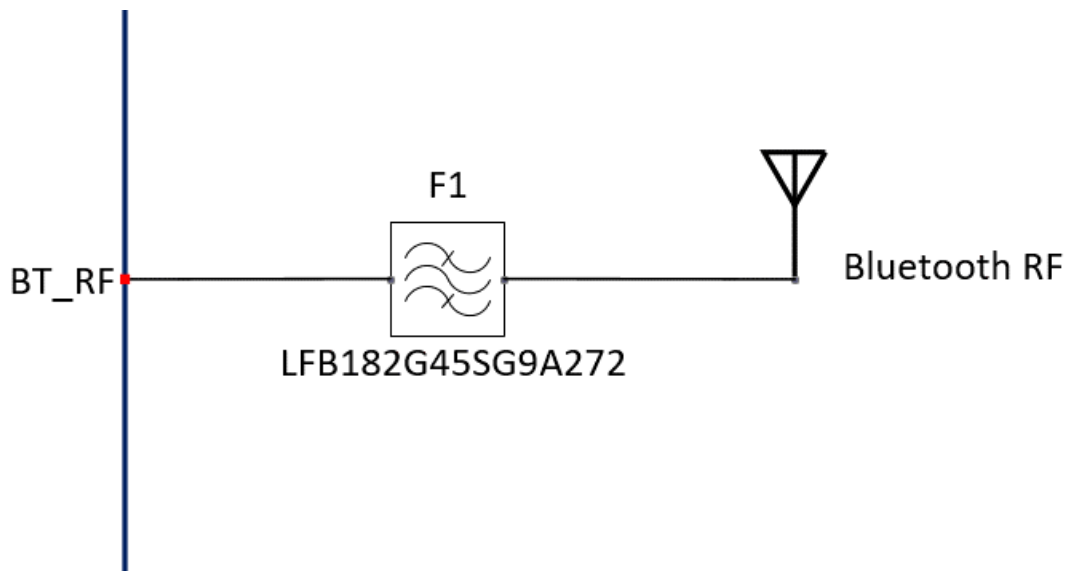


Figure 3-2 RF connection

RELATED INFORMATION

[“Recommended RF filter specification” on page 50](#)

3.3 Layout

The layout of the RF section in a QCC3084 VFBGA system can affect overall RF performance. This is even more true when it comes to ultra-miniaturized designs, where radiation issues may become more important.

Ground connections become increasingly critical at RF frequencies. All ground pins should be connected to the main RF reference ground plane (in metal layer L2) using microvias to minimize parasitic inductance. This is achieved using microvias in pad, see [Table 3-1](#) and [Figure 3-3](#).

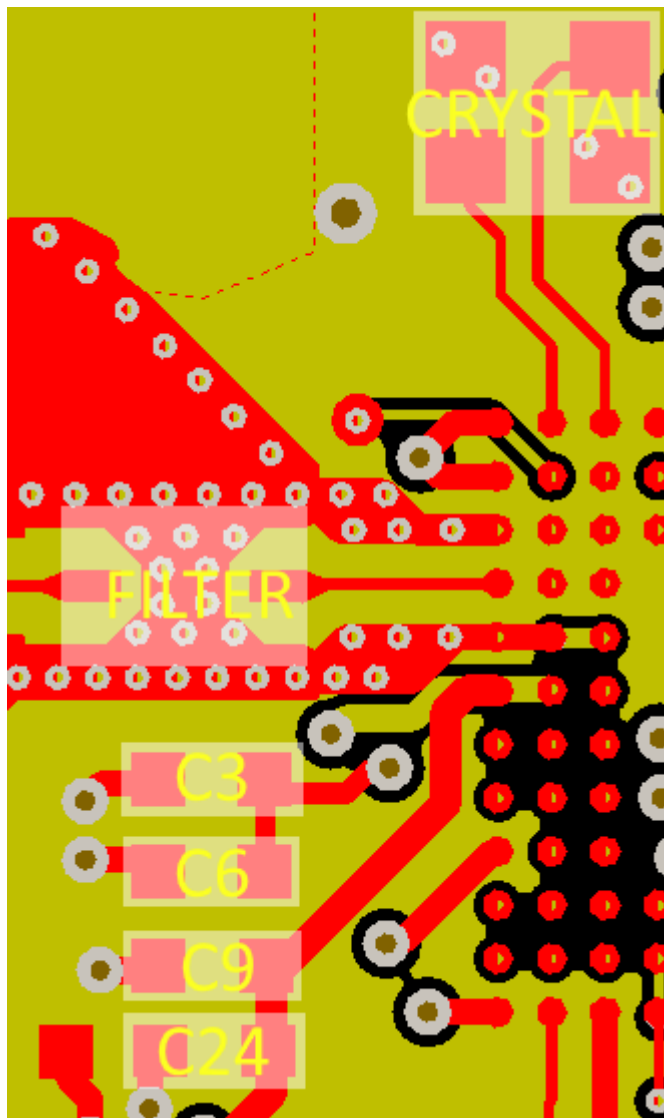
Table 3-1 QCC3084 VFBGA RF ground pins

Pin	Function	Notes
D2	RF Balun ground	Main return path for the filter and antenna path. Connect directly to the RF reference plane using a microvia.
C1	Internal baseband ground	Connect to the ground area on the side of the RF track and to the RF reference plane using a microvia.

Table 3-1 QCC3084 VFBGA RF ground pins (cont.)

Pin	Function	Notes
C2	LO ground point	Connect directly to the RF reference plane using a microvia.
C3	AUX macro GND	Connect directly to the RF reference plane using a microvia.

Figure 3-3 shows a layout snapshot of the RF and XTAL section.

**Figure 3-3 RF and XTAL layout**

The RF track is a co-planar waveguide designed to have 50 Ω impedance. The grey-colored layer is the GND plane in L2. It is important to keep the area below the RF track intact to guarantee a solid reference plane for the RF. There is no requirement to isolate this area, the L2 GND plane should extend over the whole board with the minimum amount of disruption.

The top layer RF ground is stitched to the main GND plane in L2 all along the RF track. Ground planes on different layers should be well stitched together in order to prevent resonance at RF frequencies.

NOTE Add as many of the vias as the layout will allow around the RF track.

The example in [Figure 3-3](#) shows that in the first section of the RF track before the filter, where through-hole vias cannot be used, microvias are used instead to stitch the GND planes on the top and L2 layers.

Finally, it is recommended to add GND stitching vias in the periphery of the PCB to prevent radiation from the edges of the PCB.

The band-pass filter should be located as close to QCC3084 VFBGA as possible. The grounding of the filter is critical to guarantee proper attenuation of the filter out of band.

NOTE The GND on the top layer covers the area between the two pads and this is stitched to the main GND plane in L2 with micro-vias.

[Figure 3-4](#) shows an HFSS simulation showing the improvement out of band due to this grounding strategy.

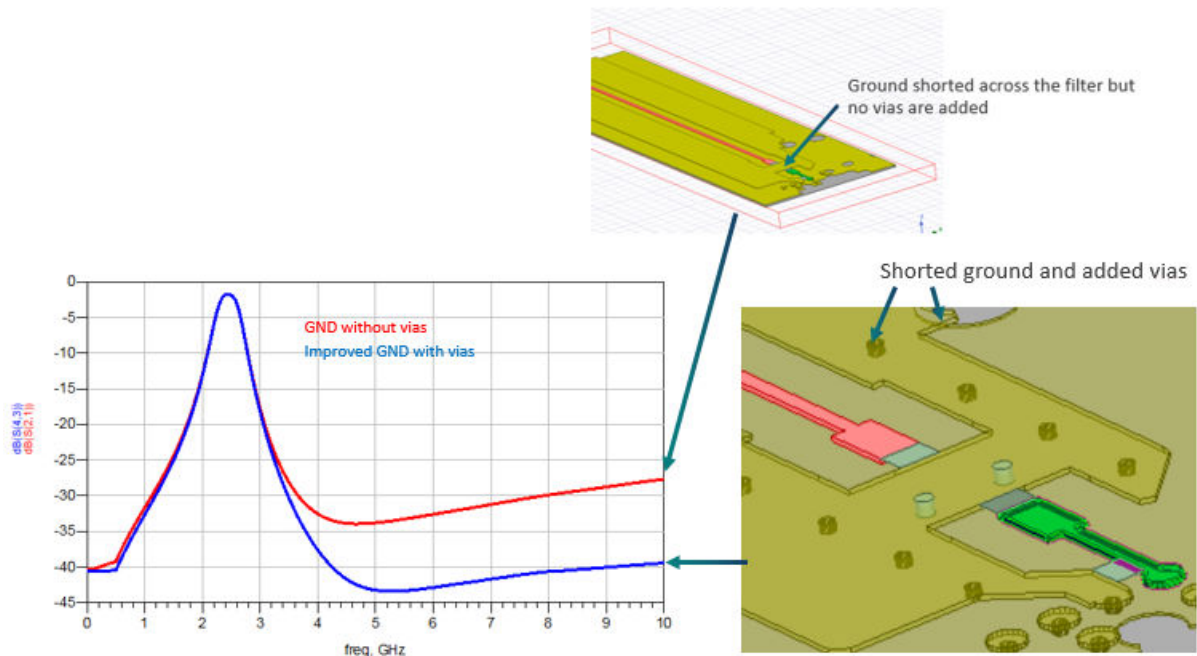


Figure 3-4 HFSS simulation showing the improvement in the out of band attenuation due to better grounding

The Crystal routing is also critical. Crystal signal harmonic coupling on a PCB can lead to receiver desense and generate spurs on transmit signals. It is therefore important to keep crystal tracks short, direct and routed away from the RF track to minimize coupling.

4 Audio

QCC3084 VFBGA has integrated analog audio, with two DACs and four ADCs. The DAC features a bridge-tied load (BTL) Class-D/AB output stage for directly driving a headset/speaker. To achieve optimal audio performance, care should be taken in audio component placement and PCB routing.

4.1 Audio bypass capacitors

The Audio macro takes the power supply (1.8 V) from VDD_AUDIO_1V8. Normally there is no need to add a decoupling cap to this supply input.

The power stage of the audio outputs is supplied from the VDD_AUDIO_HP_SPK1 and VDD_AUDIO_HP_SPK2 terminals. This should be decoupled with 1 μ F capacitors, 0402 imperial (C4 and C22 in [Figure 4-1](#)). If either the right or the left DAC channel is not used in an application the decoupling capacitor for the unused channel is not required. Because the Class-D amplifier is a switching circuit, care must be taken to route the tracks and return grounds from QCC3084 VFBGA to this capacitor before connecting to the supply planes.

The audio bandgap bypass capacitor (C20 in [Figure 4-1](#)) directly connects to the output of the audio voltage reference and current generator. This is used to remove flicker noise (also called 1/f noise). Any noise on the audio references will directly couple into the audio. This means the tracks and grounding of C20 are critical: it should be placed very close to AUDIO_BGBYP to minimize the track

length, and a correct return path to VSS_AUDIO_REF created. It should also be routed as far away from noisy traces as possible to minimize noise pickup. The optimal value is 2.2 uF 0402 imperial.

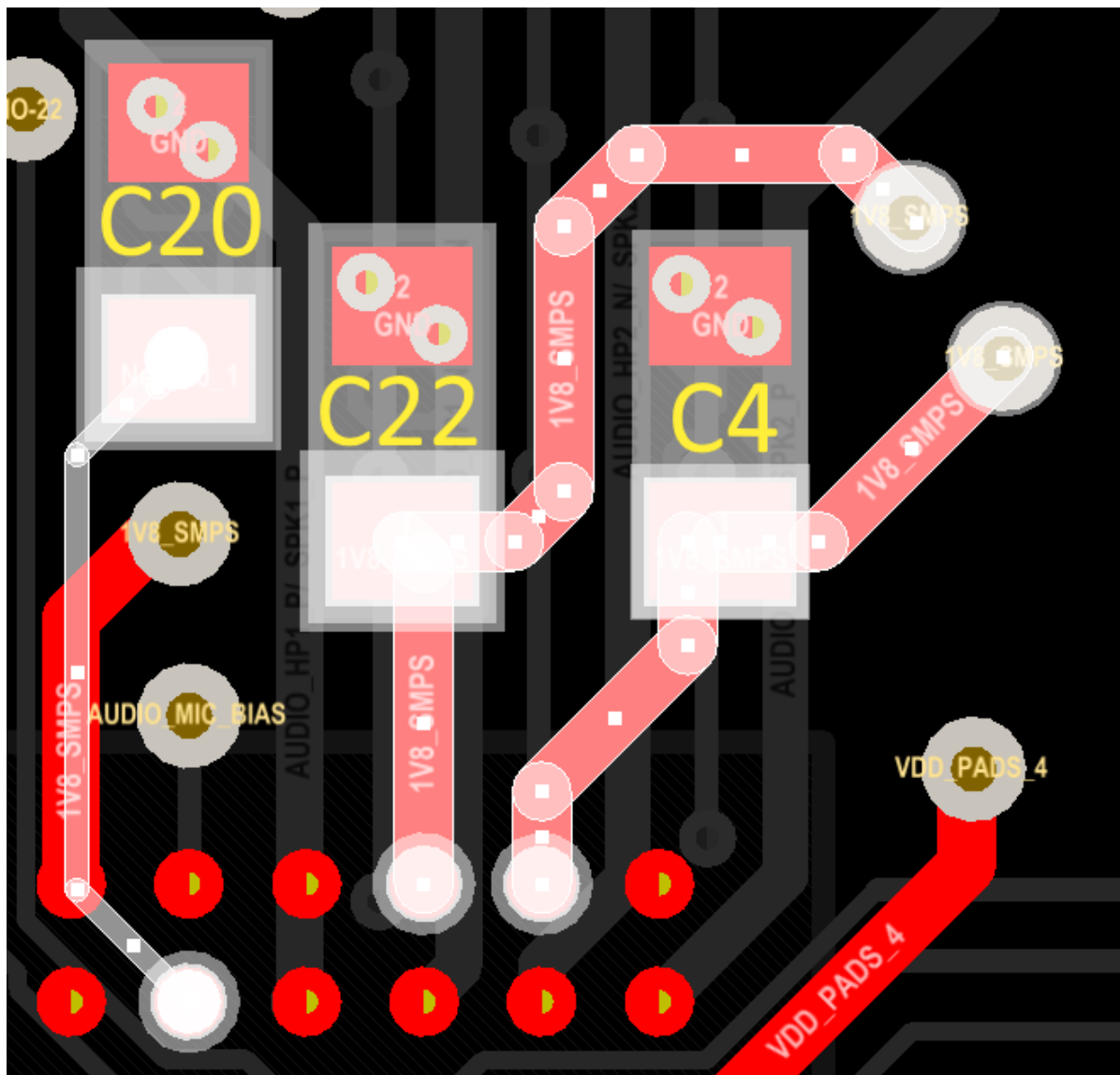


Figure 4-1 Audio layout

4.2 Headset/Speaker outputs

The QCC3084 VFBGA Class-D and Class-AB headset/speaker outputs are stereo differential outputs capable of directly driving 30 mW_{rms} into 32 Ω or 16 Ω.

Class-AB output can be used to drive high impedance loads such as line-out applications that use an external amplifier. For such applications requiring external power amplifiers, the Class-AB output should be filtered using a 30 kHz RC low pass filters as shown in the QCC3084 VFBGA example application schematic.

The outputs are routed out of AUDIO_HP1_P/SPK1_P to AUDIO_HP1_N/SPK1_N and out of AUDIO_HP2_N/SPK2_N to AUDIO_HP2_P/SPK2_P.

The recommended layout for these outputs is differential routing, keeping the two channels isolated from each other and from other sensitive circuitry.

RELATED INFORMATION

[“QCC3084 VFBGA example application schematic and BOM” on page 42](#)

4.3 Line/Mic input

For information on Line/Mic input, see *QCC3084 VFBGA Data Sheet* (80-41752-1).

4.4 Mic bias regulator

QCC3084 VFBGA incorporates a low noise linear regulator for supplying electret or MEMS microphones, with an output voltage configurable from 1.5 V to 2.1 V and maximum output current of 6 mA.

When using the mic bias regulator, mics should be powered and connected as in [Figure 4-2](#) as this will give optimal supply and interference rejection. If a capacitive load greater than 0.1 nF is required, at least 10 Ω of resistance needs to be placed between the regulator output and capacitance which can have a maximum value of 2.2 μ F. Where multiple capacitors are used the capacitance and resistance need to be split (for example, if powering 3 mics use a minimum of 30 Ω in series with a max of 0.73 μ F per mic).

See [Microphone Power supply recommendations](#) for further information on powering microphones..

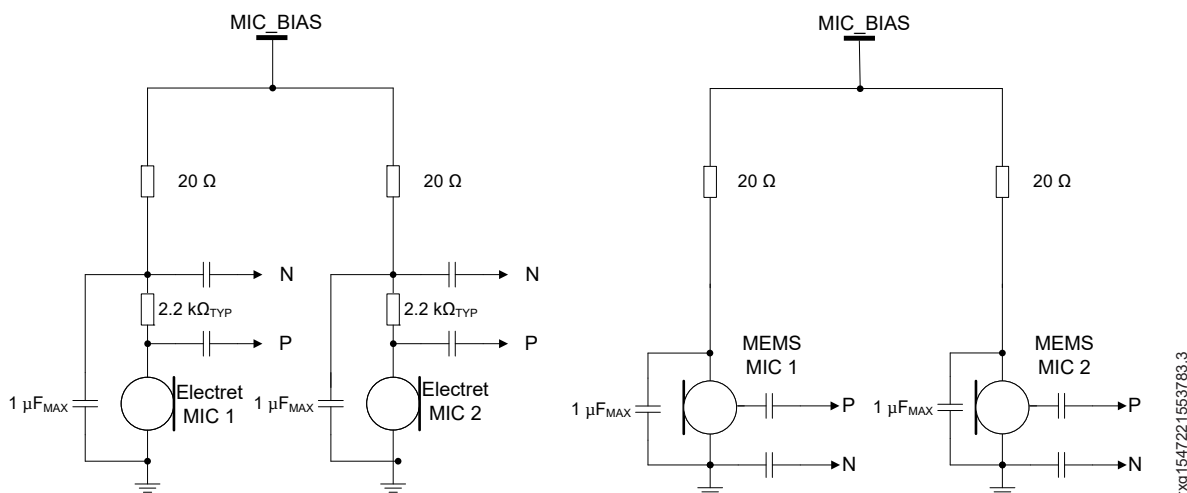


Figure 4-2 Microphone bias configuration for electret microphones (left) and MEMS microphones (right)

5 LED pads

QCC3084 VFBGA has 6 LED pads. These are configurable into four different operating modes:

1. LED driver
2. Digital/button input
3. Analog input
4. Disabled

5.1 LED driver

This mode is designed for driving LEDs. The pad is VCHG tolerant and operates as an open-drain pad. The LED cathode should be connected to the QCC3084 VFBGA LED pad.

Each pad is rated to sink up to 50 mA of current. The PCB routing should ensure that the tracking is of sufficient current capacity.

NOTE Because of the high current capability, these pads are capable of fast edge switching. The effects of noise from PWM operation of the LED's should be considered.

5.2 Digital/button input

This mode is designed for slow input signals, typically buttons. It is not designed for fast switching digital inputs like SPI. For these types of inputs, use the general PIOs.

In this mode, an internal weak pull-down can be enabled. Typically this would be used for active high button signals, to ensure the input returns to 0 when the button is released.

In this mode, the pads are VCHG tolerant and the logic '1' threshold is typically 1 V. The threshold is not well controlled. For characterized switching points, use a PIO in preference.

In digital input mode, logic inputs can be read by the software as 'virtual' PIO[63:58]. They can be used as interrupt sources in the same way as other PIOs.

5.3 Analog input

In this mode, the LED pad is used as an analog input port. The pad voltage is routable to the 10-bit auxiliary ADC.

NOTE In analog input mode, the input range is 0 to VDD_AUX_ADC. Damage may be caused if input voltages exceed 1.8 V.

5.4 Disabled

This is the default state for LED pads. The pad is VCHG tolerant and high impedance, with no pull-down.

6 Reset pin (Reset#)

The QCC3084 VFBGA digital reset pin (RESET#) is an active low reset signal. PIO[1] defaults to RESET# on boot.

When the pin is active low, on-chip glitch filtering avoids unintended resets by filtering out spurious noise. The RESET# pin has a fixed strong pull-up to VDD_PADS_1, and can be left unconnected. After boot, PIO[1] is configurable as a digital PIO.

For additional information on the Reset# pin, see *QCC3084 VFBGA Data Sheet* (80-41752-1).

7 QSPI flash interface

QCC3084 VFBGA features one quad SPI flash interface. A supported QSPI flash part must be attached to this port to store application processor code and configuration data.

For a list of supported devices, see ADK software release notes.

QSPI is a high-speed serial interface and special attention should be given to routing the signals between QCC3084 VFBGA and the flash device. QTI recommends referring to the flash manufacturers documentation for specific instructions. Generally it is advisable to match the length of clock and data lines and keep tracks as short as possible with minimum layer changes. If track length has to be increased, it is recommended to keep the impedance of traces as constant as possible and provide a reference plane for them.

If possible, the QSPI clock and data lines should be routed on internal layers with GND shielding to minimize EMI

QSPI data/clock lines should not be routed near RF circuitry or analog audio input/outputs. Ensure an unbroken ground return path.

Typically QSPI devices require a 100 nF decoupling capacitor. This should be placed next to the flash device supply pins. For further details see the flash device manufacturer recommendation.

To minimize electromagnetic interference (EMI) and optimize signal integrity it may be beneficial to individually decouple the VDD_PADS supply to the QSPI interface with 100 nF.

In designs in which the TRB interface is inaccessible it is recommended to add a 0 Ω link between the QSPI1_CS0# terminal of QCC3084 VFBGA and the chip select pin of the QSPI flash in prototype units. Temporarily removing this link allows the hardware to be reprogrammed should the code of the P1 application or MIB key configuration inadvertently block the device from enumerating on the USB bus.

When operating the QSPI memory interface at a clock frequency of 80 MHz, additional attention should be given to the routing of the traces between QCC3084 VFBGA and the memory. All traces should be routed as a high-speed bus with controlled impedance traces (typically 50 Ω). The clock line should be kept a minimum of 3 times the trace width away from the data lines. Where possible, a continuous reference plane should be provided on adjacent layers with via stitching.

Ground loop parasitics should be kept as low as possible. It is recommended to have multiple ground vias on both sides of the high-speed bus. If staggered micro vias is preferred, then multiple micro vias per layer on the ground return paths should be used if possible.

8 USB interfaces

QCC3084 VFBGA has one USB device interface (an upstream port, for connection to a host phone/PC or battery charging adaptor).

8.1 USB device port

The device port is a full speed (12 Mb/s) port. Typically, QCC3084 VFBGA enumerates as a compound device operating as a hub. The enabled audio source / sink / HID / mass storage device appears behind this hub.

The DP 1.5 k pull-up is integrated in QCC3084 VFBGA. No series resistors are required on the USB data lines.

The VCHG input of QCC3084 VFBGA is tolerant of a constant 6.5 V and transients up to 7.0 V. If extra overvoltage protection is required, external clamping protection devices can be used.

For system level ESD protection on USB pins, see *Related Information*.

RELATED INFORMATION

[“System level ESD protection” on page 39](#)

8.1.1 USB connections

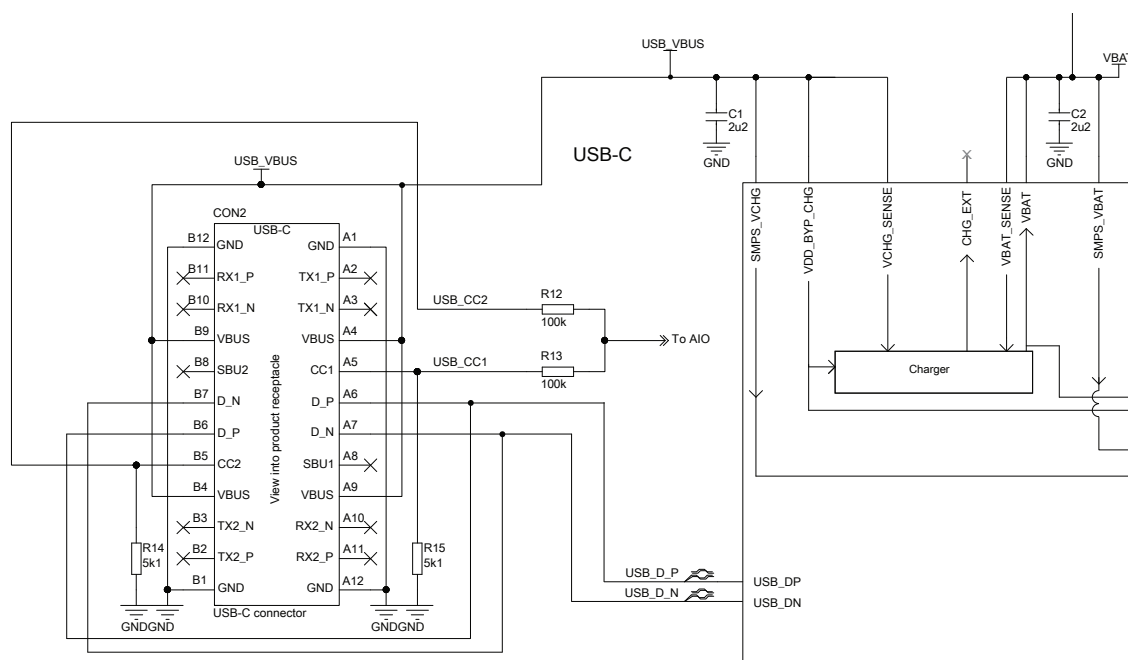


Figure 8-1 Standard USB Type-C®

All USB standards and connectors are specified to ensure that the Ground connection is made first and breaks last, ensuring a correct and stable ground reference for charger detection and USB communications.

Any non-standard (for example pogo pins or snap contact connectors) should be designed in the same way to ensure a good ground connection is maintained reliably, such as positioning a ground connection at either end to ensure that a slightly lifted connection still maintains a ground connection.

This is particularly important if the other end of the USB cable is made available as a standard type A or C connector which could be used with alternative chargers by the end user. There is a risk that a USB connection with intermittent ground connection or missing ground connection could be mis-interpreted by some alternative chargers as a command to increase their VBUS voltage to higher voltages, leading to damage of the downstream device.

QCC3084 VFBGA is USB 2.0 full speed only. It can simply connect to the central data pins, and the four VBUS pins of the USB-C® connector. The connector ensures correct connection in either orientation. Unused connector pins should be left nonconnected.

For simple charger detection of 1.5 A and 3.0 A capable chargers, the two USB CC lines can be individually terminated with the required 5.1 k resistor, then a single LED/AIO input can be used by high impedance combination to sense the CC line voltage thresholds.

Charging only USB port

Connect VCHG and VBUS as in [Figure 8-1](#). Leave the USB_DP and USB_DN pins unconnected. This allows USB charger detection to complete and enter the 'Data lines Floating' charger type.

No USB connection

Leave USB_DP and USB_DN pins unconnected.

8.1.2 Layout notes

QCTL recommends keeping USB data line tracks between the connector and QCC3084 VFBGA as short as possible, with minimum layer changes, and a continuous ground path beneath the data tracks.

Over longer distances, USB data lines should be routed as a 90 Ω differential pair. They should have a single ended impedance to ground of around 45 Ω and a track length matched to avoid skew.

Route USB tracks away from the RF and crystal sections of the system to avoid interference.

Stubs on the data lines should be avoided and kept to a minimum where unavoidable, such as USB-C connectors.

RELATED INFORMATION

[“Charger” on page 18](#)

8.1.3 USB charger detection

QCC3084 VFBGA supports charger detection to the USB BCv1.2 standard. It provides data contact detection (DCD) using an internal current source, and provides:

- Detection of standard downstream ports (SDP)
- Charging downstream ports (CDP)
- Dedicated downstream ports (DCP).

Secondary detection is not supported. Detection of accessory charger adapter (ACA) using ID pin resistance could be implemented by routing the ID pin to a suitable analog input and appropriate application code.

Chargers using USB-C CC line advertising can be detected by reading the CC line voltage.

The voltage on the USB data lines can be read by a 10-bit auxiliary ADC. This is also used for the AIO pad measurements and enables detection of proprietary chargers which voltage bias the USB data lines. For additional information about proprietary charger types, refer to the ADK configuration tool.

9 System level ESD protection

Sufficient system level ESD protection is critical to develop reliable products. The required protection devices and their location depend on both the electrical and mechanical design of a product. External devices such as TVS diodes are generally required on terminals that are exposed to the end user as well as components mounted behind apertures in the product enclosure. If TVS diodes are used, they should be placed between signal traces and grounded to limit ESD induced voltages/currents and to protect QCC3084 VFBGA.

The following devices/interfaces typically require adding protection devices:

- USB
- Speaker driver
- Microphone
- Line input
- Push button

Figure 9-1, Figure 9-2, Figure 9-3, Figure 9-4, and Figure 9-5 show examples of adding protection devices to USB, speaker, microphone, line input, and push button.

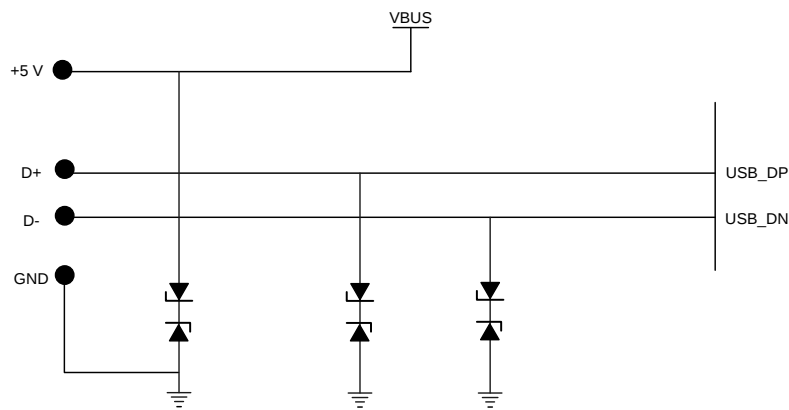


Figure 9-1 ESD protection for USB

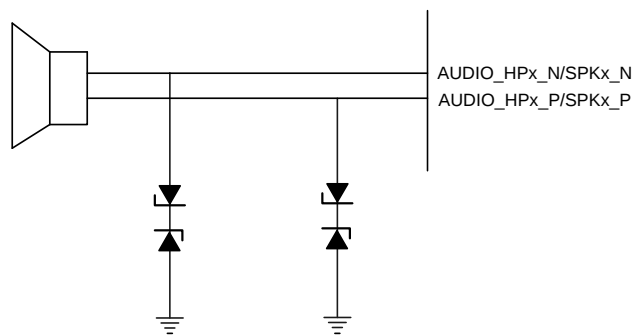


Figure 9-2 ESD protection for speaker

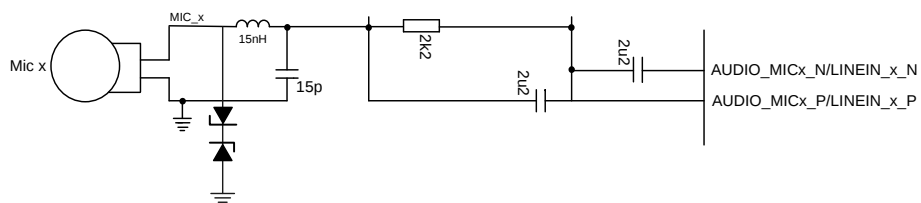


Figure 9-3 ESD protection for microphone

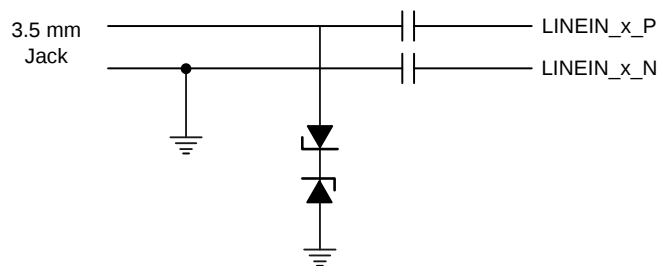


Figure 9-4 ESD protection for line input

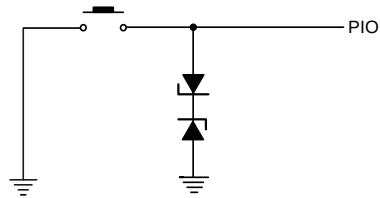


Figure 9-5 ESD protection for push button

TVS diodes act as a capacitor when not being activated by an ESD event. Care should be taken when selecting parts to protect high speed or switching interfaces such as USB, digital microphone interfaces, and Class-D headphone outputs. Capacitance should be minimized as it may impact signal integrity and cause additional power consumption.

Additionally, QCC3084 VFBGA incorporates device level ESD protection into all terminals, which is intended to protect the device through the manufacturing and PCB assembly process. For further details, see *QCC3084 VFBGA Data Sheet* (80-41752-1).

A QCC3084 VFBGA example application schematic and BOM

QCC3084 VFBGA example application schematic

Figure A-1 shows the example application schematic for QCC3084 VFBGA.

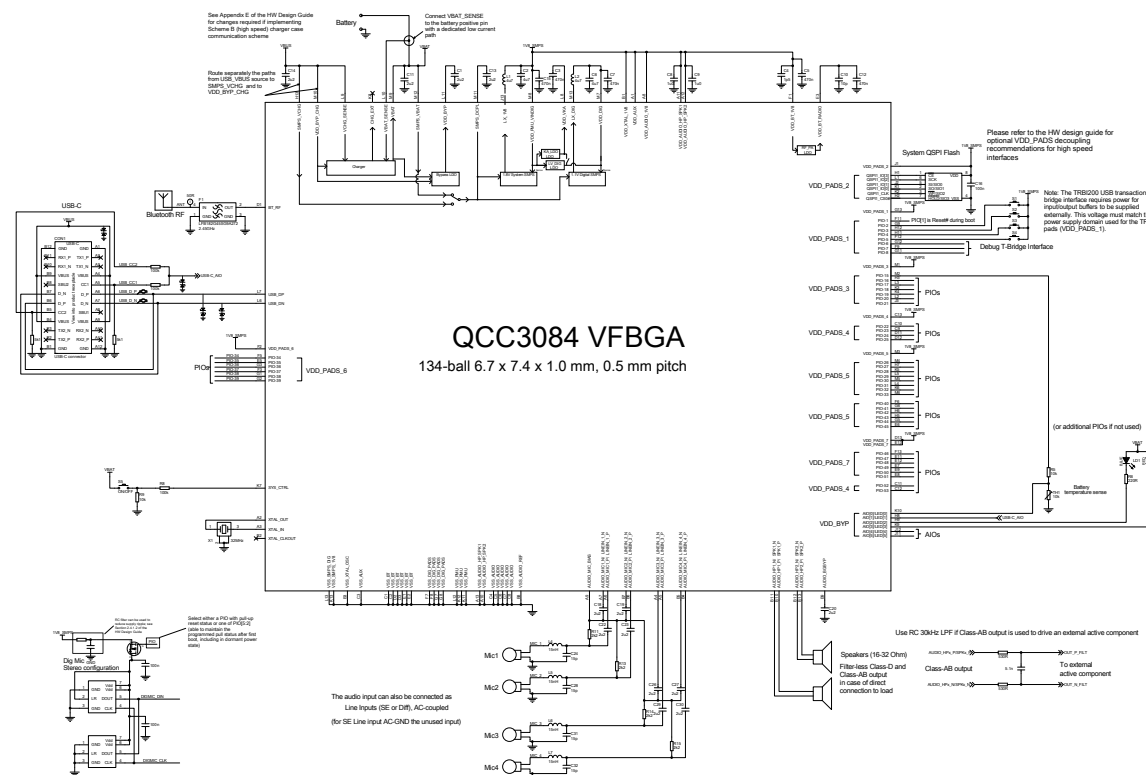


Figure A-1 QCC3084 VFBGA example application schematic

QCC3084 VFBGA bill of materials

[Table A-1](#) lists the bill of materials (BOM) of the system components for the QCC3084 VFBGA example application schematic shown in this document.

For more information about QCC3084 VFBGA, see *QCC3084 VFBGA Data Sheet* (80-41752-1).

Table A-1 QCC3084 VFBGA bill of materials

Item No.	Qty Req.	Circuit Ref.	Description	Value	Tolerance	Voltage	Material	Package (metric) ^a	Manufacturer	Manufacturers Part No.
1	1	U1	QCC3084 VFBGA 134-ball 6.7 x 7.4 x 1.0 mm 0.5 mm pitch	QCC3084 VFBGA	-	-	-	VFBGA 134-ball 6.7 x 7.4 x 1.0 mm 0.5 mm pitch	QTIL	QCC-3084-0-CSP134ATR-05-0
2	1	U7	1.8 V 128 Mb Serial flash memory with dual / quad SPI	W25Q128 JWSIQ	-	-	-	8-SOIC	Winbond	W25Q128JWSIQ
3	1	F1	Filter Murata 2.45 GHz band pass chip filter	2.45 GHz	-	-	-	FILTER MURATA LFB182G4	Murata	LFB182G45SG9A272
4	1	X1	Crystal	32 MHz	10 ppm	-	-	2016	Murata	XRCGB32M000F1S2JR0
5	11	C1, C11, C18, C19, C20, C22, C23, C26, C27, C29, C30	Capacitor	2.2 μ F	10%	6.3 V	X5R	1005	Taiyo Yuden	JMK105BJ225KV-F
6	2	C13, C14	Capacitor	2.2 μ F	10%	16 V	X5R	1005	Murata	GRM155R61C225KE11J
7	1	C4	Capacitor	1.5 pF	0.25 pF	25 V	C0G	0603	TDK	C0603C0G1E1R5CT00NN
8	5	C3, C5, C7, C12, C15	Capacitor	470 nF	20%	4 V	X5R	0603	Murata	GRM033R60G474ME90
9	2	C8, C9	Capacitor	1.0 μ F	10%	6.3 V	X5R	1005	Murata	GRM155R60J105KE19J
10	1	C10	Capacitor	10 pF	2%	25 V	C0G	0603	Murata	GRM0335C1E100GA01D
11	1	C16	Capacitor	100 nF	10%	6.3 V	X5R	0603	Murata	GRM033R60J104KE19D
12	2	C2, C6	Capacitor	4.7 μ F	20%	10 V	X5R	1005	Murata	GRM155R61A475MEAAD
13	2	L1, L2	Inductor	4.7 μ H	20%	-	Multilayer Ferrite	2016	Murata	DFE201610E-4R7M

Table A-1 QCC3084 VFBGA bill of materials (cont.)

Item No.	Qty Req.	Circuit Ref.	Description	Value	Tolerance	Voltage	Material	Package (metric) ^a	Manufacturer	Manufacturers Part No.
14	1	R9	Resistor	10 kΩ	5%	-	Thick Film	0603	Phycomp	2322 803 70103L
15	1	R8	Resistor	100 kΩ	5%	-	-	-	-	-

^a 1005 (metric) / 0402 (imperial), 0603 (metric) / 0201 (imperial), 2016 (metric) / 0806 (imperial).

B Recommended SMPS components specification

B.1 Inductor specification

Table B-1 lists SMPS information relevant to the inductor choice.

Table B-1 SMPS inductor specification

Parameter	1.8 V SMPS	Digital SMPS
Output Voltage	1.8 V	0.7/0.8/0.9 V
Operation Modes	PWM, PFM, ULP	
PWM frequency	2 MHz	
PFM / ULP frequency	Dependent on load	
PWM max load current	350 mA	250 mA
Max inductor current in PWM mode	Max load current + 100 mA	
PFM / ULP max load current	40 mA	55 mA
Max inductor current in PFM/ULP modes	350 mA (independent of load)	
Minimum inductor saturation current (current limit operational). Note: The inductor saturation current is the point where the inductance is 30% below the nominal value. This is not the inductor rated current. Note: QTIL recommends to use inductors with a minimum saturation current rating that is at least 30% higher than the target Max inductor current in PWM mode.	600 mA	500 mA
Nominal inductor value	4.7 μ H ($\pm$ 20%)	
Inductor ESR / DCR	290 m Ω , lower values are preferred for SMPS efficiency	

B.2 Recommended inductors

The parts in [Table B-2](#) meet the specification detailed in this document and have been tested by QTIL.

Table B-2 SMPS recommended inductors

Manufacturer	Case (metric)	Part number
Murata	2016	DFE201610E-4R7M=P2
Taiyo Yuden	1608	MBKK1608T4R7M
Cyntec	1210	HTQX12100H-4R7MSR-11
CoilCraft	1608	PFL1609-472ME
Cyntec	2012	HTQH2012FE-4R7MSR-11

B.3 SMPS capacitor specification

[Table B-3](#) lists the SMPS capacitor specification.

Table B-3 SMPS capacitor specification

Parameter	SMPS_DCPL 2.2 μ F	1.8 V SMPS 4.7 μ F	Digital SMPS 4.7 μ F
Dielectric	X5R / X7R		
Package Size	0402 (imperial) / 1005 (metric) or 0201 (imperial) / 0603 (metric)		
Tolerance	$\pm 20\%$		
Max DC voltage derate	<60% @ 5 V	<20% @ 1.8 V	<20% @ 0.9 V
Rated voltage	≥ 10 V	≥ 4.0 V	
Max ESR	<50 m Ω		

C Recommended crystals specification

This section describes the key specification requirements for crystals to be used with QCC3084 VFBGA.

RELATED INFORMATION

[“Layout” on page 26](#)

C.1 Electrical requirements

[Table C-1](#) lists performance to be met over operating temperature range unless otherwise stated.

Table C-1 Electrical requirements

Parameter	Description	Min	Typ	Max	Units	Notes
F _{nom}	Nominal fundamental frequency	-	32	-	MHz	-
C _P	Package capacitance (32 MHz)	-	1	2	pF	-
C _L	Load capacitance	-	6	10	pF	-
F _{tol_nom}	Frequency tolerance nominal	-10	-	10	ppm	At 25°C±3°C
F _{tol_temp}	Frequency stability over temperature	-10	-	10	ppm	Over specified temperature range with respect to frequency error at nominal
F _{tol_aging}	Frequency tolerance with aging @ Ta = 25°C±3°C	-1	-	1	ppm/yr	1 st year
F _{tol_aging_10yrs}	Total frequency tolerance with aging over 10 years	-10	-	10	ppm	-
ESR	Motional Resistance (32 MHz)	-	25	50	Ω	-
Drive Level	DL	-	100	200	μW	-

C.2 Recommended crystals

The parts in [Table C-2](#) meet the specification detailed in this document and have been tested by QTIL. Customers should satisfy themselves that the oscillator has sufficient margin in their design with any crystal resonator they select.

Table C-2 QCC3084 VFBGA recommended crystals

Frequency	Temp. range	Package	Manufacturer	Part Number
32 MHz	-30°C / 85°C	2016	Murata	XRCGB32M000F1S2JR0
32 MHz	-30°C / 85°C	2016	TXC	8Y32072003
32 MHz	-30°C / 85°C	1612	TXC	9Q32072001
32 MHz	-30°C / 85°C	2016	Siward	XTL501-Q23-045
32 MHz	-30°C / 85°C	1612	Siward	XTL901-Q23-046

D Recommended RF filter specification

This section describes the key specification requirements for radio frequency (RF) band pass filters for QCC3084 VFBGA applications.

NOTE Correct PCB layout is critical to achieve the datasheet performance of LTCC band pass filters.

RELATED INFORMATION

[“RF filter” on page 26](#)

D.1 Electrical requirements

[Table D-1](#) lists performance to be met over operating temperature range unless otherwise stated.

Table D-1 Electrical requirements

Parameter	Frequency (MHz)	Min	Typ	Units	Notes
Characteristic impedance		-	50	Ω	
Attenuation	4800 to 5000 (second harmonic)	26	-	dB	
	7200 to 7500 (third harmonic)	18	-	dB	
	1200 to 1250	12	-	dB	
	1800 to 1875	5	-	dB	
	3000 to 3125	5	-	dB	
	3600 to 3750	15	-	dB	
	5400 to 5625	14	-	dB	
	9600 to 10000	20	-	dB	
	12000 to 12500	13	-	dB	

D.2 Recommended radio frequency filters

Table D-2 lists recommended RF filters for use with QCC3084 VFBGA devices.

Table D-2 QCC3084 VFBGA recommended radio frequency filter parts

Frequency	Temp. range	Package	Manufacturer	Part Number
2400 to 2500 MHz	-40°C / 85°C	1.6 x 0.8 x 0.6 mm	TDK	DEA162450BT-1295A1
2400 to 2500 MHz	-40°C / 85°C	1.6 x 0.8 x 0.7 mm	Murata	LFB182G45SG9A272
2400 to 2500 MHz	-40°C / 105°C	1.1 x 0.9 x 0.6 mm	Walsin	RFBPF1109060A28Q1C

E Charger case communication

Qualcomm supports two case-earbud communication schemes using just the VCHG and GND connections to pass information between a charger case and earbuds. Scheme A provides up to 1 kb/s and Scheme B provides up to 1.5 Mb/s symbol rate. Different hardware configurations are required for the two schemes, so an implementation can support one scheme for a given hardware configuration. The schemes are not intended to be mixed in the same application.

Qualcomm Scheme A case-earbud communications scheme does not require any additional components in the earbud.

The higher data rate Qualcomm Scheme B case-earbud communications scheme requires additional routing and components in the earbud. See [Figure E-1](#) and [Table E-1](#).

See *Qualcomm Charger Case Communication Specification* (80-21985-1) for full details of these schemes, and associated hardware and software.

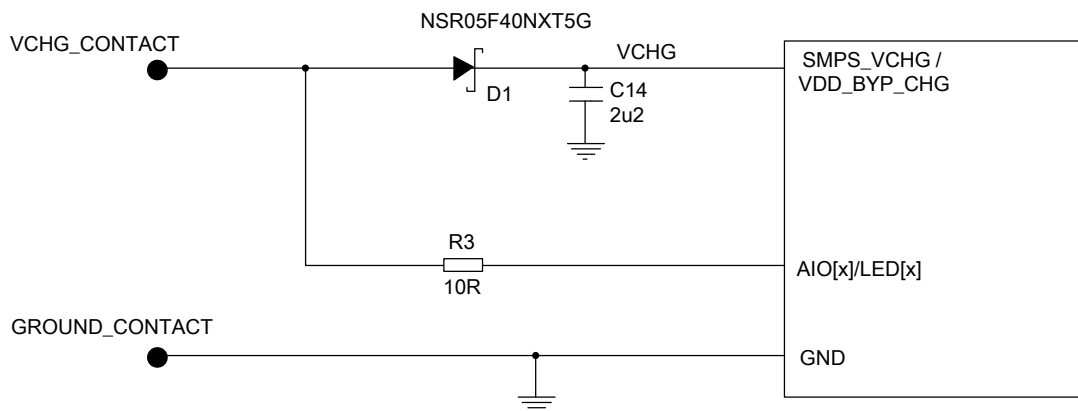


Figure E-1 Additional circuitry for Qualcomm Scheme B case-earbud communications

Table E-1 Additional example BOM components for Qualcomm Scheme B case-earbud communications

Item No.	Qty Req.	Circuit Ref.	Description	Value	Tolerance	Voltage	Material	Package	Manufacturer	Manufacturers Part No.
1	1	D1	500 mA Schottky diode. Vf 460 mV @ 500 mA	NSR05F40NXT5G	-	-	-	DSN2 (1.0 x 0.6 mm)	On Semi	NSR05F40NXT5G
2	1	R3	Resistor	10Ω	5 %	-	-	-	-	-

The example D1 component above is suitable for charge currents up to 500 mA.

Resistor R3 is placed to add protection to the LED pad, but it is not guaranteed to protect the LED pad if it is inadvertently set to drive 0 while VCHG is powered at 5 V. Care should be taken during software development. The LED pad used for case communications can be configured.

Capacitor C14 is the VCHG pin capacitor required with or without case communications.

Depending on end product design, additional ESD protection may be required to protect the LED pin and diode from ESD damage. Any ESD components used must be low capacitance to avoid loading the VCHG_CONTACT net and slowing communications.

Document references

Document	Reference
<i>QCC3084 VFBGA Data Sheet</i>	80-41752-1
<i>Qualcomm Charger Case Communication Specification</i>	80-21985-1

Glossary

Term	Definition
ACA	Accessory charger adapter
AIO	Analog input/output
Bluetooth	Set of technologies providing audio and data transfer over short-range radio connections
BOM	Bill of materials
BTL	Bridge-tied load
ECM	Electret Condenser Microphone
EMI	Electromagnetic interference
IC	Integrated circuit
I ² C	Inter-integrated circuit interface
I ² S	Inter-integrated circuit sound
LDO	Low (voltage) drop-out
LED	Light-emitting diode
LTCC	Low temperature co-fired ceramic
MEMS	Micro electro mechanical system
PCB	Printed circuit board
PCM	Pulse code modulation
PDM	Pulse-density modulation
PFM	Pulse frequency modulation
PIO	Programmable input/output, also known as general-purpose I/O
ppm	parts per million
PWM	Pulse width modulation
QSPI	Quad serial peripheral interface (flash)
QTI	Qualcomm Technologies International, Ltd.
RF	Radio frequency
SAW	Surface acoustic wave

Term	Definition
SMPS	Switch-mode power supply
SPI	Serial peripheral interface
UART	Universal asynchronous receiver transmitter
USB	Universal serial bus
WLCSP	Wafer level chip scale package
XTAL	Crystal